REMARKS/ARGUMENTS

Reconsideration and allowance of this application are respectfully requested. Currently, claims 1 and 4 are pending in this application.

Rejection Under 35 U.S.C. §103:

Claims 1-3 were rejected under 35 U.S.C. §103 as allegedly being unpatentable over Applicant admitted prior art and Yamaguchi (EP 0853378 A2). Applicant respectfully traverses this rejection with respect to still pending claim 1.

In order to establish a prima facie case of obviousness, all of the claimed limitations must be taught or suggested by the prior art. Applicant submits that the combination of admitted prior art and Yamaguchi fails to teach or suggest all of the claimed limitations. For example, the combination fails to teach or suggest "wherein said temperature characteristic compensating circuit includes an NPN bipolar transistor having a conductive terminal connected to the base of said PNP bipolar transistor, and said PNP and NPN bipolar transistors are packaged into a dual transistor," as required by independent claim 1.

Yamaguchi discloses a circuit in which a first bipolar transistor for supplying a constant voltage to the drain of a transistor for frequency conversion and a second bipolar transistor for canceling a temperature characteristic of the first bipolar transistor have the same polarity (see Figs. 1, 5 and 6 of Yamaguchi). In contrast, claim 1 requires first and the second bipolar transistors being implemented by the PNP and NPN bipolar transistors, respectively. The polarity

of the bipolar transistors of claim 1 are therefore different from each other. The configuration of the converter required by claim 1 is thus different from that of the circuit of Yamaguchi. The admitted prior art fails to remedy this deficiency of Yamaguchi.

Moreover, Yamaguchi discloses that when an integrated circuit including two PNP bipolar transistors in a single chip is used, it is possible to obtain two PNP transistors (i.e., same polarity transistors) having substantially the same characteristics (see page 5, lines 55-57 of Yamaguchi). Meanwhile, in the invention according to claim 1, two bipolar transistors each having different polarity are packaged into one dual transistor. The temperature condition can therefore be the same for each of the two bipolar transistors, and further, the area occupied by the transistor within the circuit can be reduced by the packaging. Advantageous effects such as weight reduction of devices due to space savings can thus be obtained by the present invention (see page 7, lines 26-32 of the originally-filed specification). The admitted prior art and/or Yamaguchi fail to appreciate these advantages.

Accordingly, Applicant submits that claim 1 is not "obvious" over the admitted prior art and Yamaguchi. Applicant therefore requests that the rejection of this claim under 35 U.S.C. §103 be withdrawn.

New Claim:

New claim 4 has been added to provide additional protection for the invention. New claim 4 requires a mixer having "a temperature characteristic compensating circuit for canceling a temperature characteristic of the PNP bipolar transistor, the temperature characteristic compensating circuit including an NPN bipolar transistor having a conductive terminal connected to a base of said PNP bipolar transistor." Applicant submits that claim 4 is allowable.

Conclusion:

Applicant believes that this entire application is in condition for allowance and respectfully requests a notice to this effect. If the Examiner has any questions or believes that an interview would further prosecution of this application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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